

METHOD FOR MANUFACTURING SPLIT-GATE EEPROM
MEMORY CELL AND STRUCTURE FORMED THEREBY

ABSTRACT OF THE DISCLOSURE

- 5 A method for producing a self-aligned split-gate EEPROM memory cell is provided. The memory cell has a cell size smaller than the traditional spilt-gate structure without sacrificing program disturb immunity. Moreover, the program current of the memory cell is much lower than the stack-gate structure. The method includes steps of:
- 10 providing a silicone substrate, forming a select gate on the silicone substrate, growing a tunnel oxide layer on exposed surfaces of the silicon substrate, forming a floating gate self-aligned to one side of the select gate, performing an ion implantation to form a source region and a drain region on the silicone substrate, and forming a control gate over the
- 15 floating gate and the select gate, wherein the control gate, the floating gate and the select gate are insulated from one another.

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